

ABSTRACT OF THE DISCLOSURE

There is provided a clock multiplication circuit simple in configuration, easy to adjust the characteristics thereof, and capable of shortening lockup time. The clock multiplication circuit is a circuit for delivering an output clock signal at a frequency that is a multiple of the frequency of a reference clock signal as inputted. A counter of the circuit counts the number of rising edges of the output clock signal ST existing during a High level period of the reference clock signal SR, thereby delivering a count value CN. A subtracter subtracts the count value CN from a reference value BN, thereby delivering a difference value DN. An adder adds the difference value DN to a preceding integrated value IN, thereby calculating a new integrated value IN. A DA converter delivers the analog control voltage AV corresponding to the integrated value IN. A VCO delivers the output clock signal ST at a frequency corresponding to the analog control voltage AV. With the circuit, the frequency of the output clock signal ST is controlled such that $DN = BN - CN = 0$.